

## Chapter 16 Built-in high speed counter of GM6-CPUC

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## **16. Built-in high speed counter of GM6-CPUC**

### **16.1. Introductions**

This chapter describes the specification, handling, and programming of built-in high speed counter of GM6-CPUC module. The built-in high speed counter of GM6-CPUC (Hereafter called HSC) has the following features;

- 3 counter functions as followings
  - 1-phase up / down counter : Up / down is selected by user program
  - 1-phase up / down counter : Up / down is selected by external B phase input
  - 2-phase up / down counter : Up / down is automatically selected by the phase difference between phase A and B.
- Multiplication (1, 2, or 4) with 2-phase counter
  - 2-phase pulse input multiplied by one : Counts the pulse at the leading edge of phase A.
  - 2-phase pulse input multiplied by two : Counts the pulse at the leading / falling edge of phase A.
  - 2-phase pulse input multiplied by four : Counts the pulse at the leading / falling edge of phase A and B

**16.2. Performance specifications**

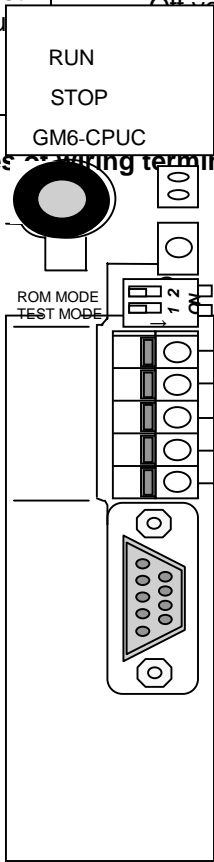
Items		Specifications
Input signal	Types	Phase A, Phase B, Preset
	Rated level	24VDC (13mA)
	Signal type	Voltage input
Counting range		0 ~ 16,777,215 (Binary 24 bits)
Max. counting speed		50k pps
Up / Down selection	1-phase	Sequence program or B-phase input
	2-phase	Auto-select by phase difference of phase A and B
Multiplication		1, 2, or 4
Preset input		Sequence program or external preset input

**16.3. Input specifications**

**16.3.1. Function of input terminals**

Items		Specifications
A / B phase	Rated input	24VDC (13mA)
	On voltage	14VDC or higher
	Off voltage	2.5VDC or lower
Preset input	Rated input	24VDC (10mA)
	On voltage	19VDC or higher
	Off voltage	6V or lower
	Delay time	Less than 1.5ms
	Delay time	Less than 2ms

**16.3.2. Names of wiring terminals**



No. of terminal	Input signal
1	A phase input
2	B phase input
3	COM
4	Preset input
5	Preset COM

16.3.3. External interface circuit

	Internal circuit	No. of terminal	Signal type	Operation voltage	
Input		1	A-phase pulse input 24VDC	ON	14 ~ 26.4 VDC
		2	B-phase pulse input 24VDC	OFF	Less than 2.5VDC
		3	COM		
Input		4	Preset input 24V	ON	19 ~ 26.4 V
		5	Preset COM	OFF	6 V □□

**16.4. Wiring**

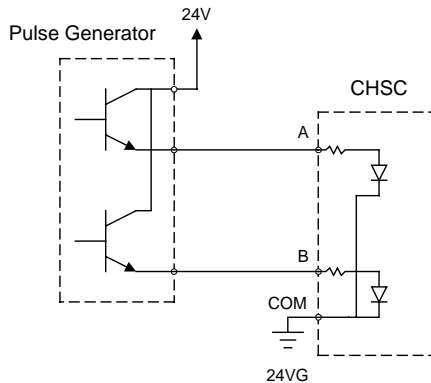
**16.4.1. Wiring instructions**

A high speed pulse input is sensitive to the external noise and should be handled with special care. When wiring the built-in high speed counter of GM6-CPUC, take the following precautions against wiring noise.

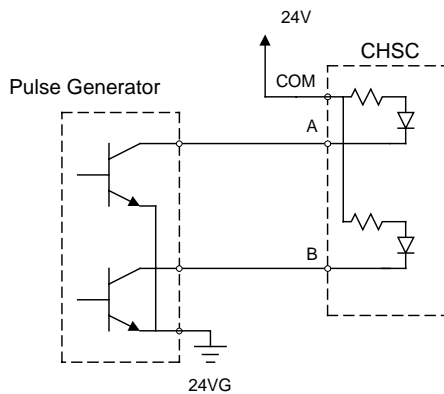
- 1) Be sure to use shielded twisted pair cables. Also provide Class 3 grounding.
- 2) Do not run a twisted pair cable in parallel with power cables or other I/O lines which may generate noise.
- 3) Before applying a power source for pulse generator, be sure to use a noise-protected power supply.
- 4) For 1-phase input, connect the count input signal only to the phase A input; for 2-phase input, connect to phases A and B.

**16.4.2. Wiring examples**

1) Voltage output pulse generator



2) Open collector output pulse generator



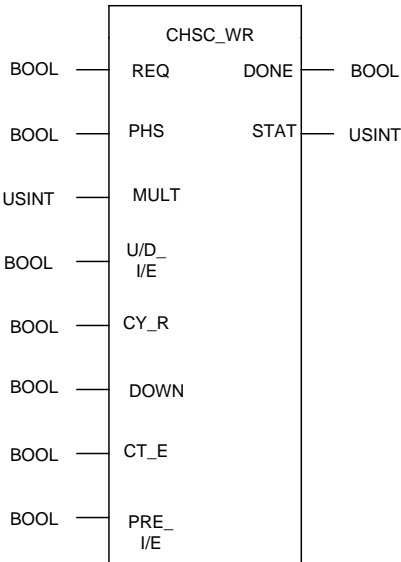
**16.5. Programming**

**16.5.1. Function block (F/B)**

**CHSC\_WR**

**CHSC\_WR**

GM1	GM2	GM3	GM4	GM5	GM6
					●

FUNCTION BLOCK	Description
	<p><b>Input</b></p> <p>REQ : Request signal of F/B execution</p> <p>PHS : Operation modes selection 0 (1-phase counter), 1(2-phase counter)</p> <p>MULT : Assign the multiplication factor (MULT = 1, 2, or 4)</p> <p>U/D_I/E : Assign the count direction (up/down) selector 0 : Set by sequence program 1 : Set by B-phase input signal (1:up-count, 0:down-count)</p> <p>CY_R : Carry reset signal ( 1: reset).</p> <p>DOWN : Select the count direction (0:up/1:down) when the counter is set as 1-phase counter and up/down is selected by sequence program. (PHS=0 &amp; U/D_I/E=0)</p> <p>CT_E : Counter enable signal (0 : Counter disable, 1 : Enable)</p> <p>PRE_I/E : Assign PRESET input 0 : PRESET by sequence program 1 : PRESET by external input at the PRESET terminal</p> <p><b>Output</b></p> <p>DONE : Turns on after the F/B is executed with no error.</p> <p>STAT : Indicate the operation status of F/B</p>

- The MULT input will be dummy input when the HSC is set as 1-phase counter (PHS = 0). When the HSC is set as 2-phase counter, the U/D\_I/E and DOWN input will be dummy input. (PHS = 1)
- The current value of HSC will be cleared as 0 when the CT\_E (counter enable) is 0.

# CHSC\_RD

Read the current value and operation status of HSC

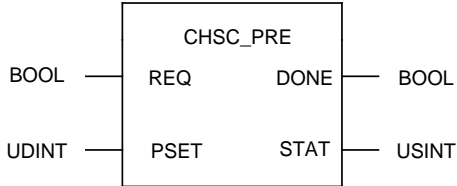
GM1	GM2	GM3	GM4	GM5	GM6
					●

FUNCTION BLOCK	Description
	<p><b>Input</b> REQ : Request signal for F/B execution</p> <p><b>Output</b></p> <p>DONE : Turns on after the F/B is executed with no error.</p> <p>STAT : Indicates the operation status of F/B</p> <p>CNT : The current value of HSC (0 ~ 16,777,215)</p> <p>CY : Carry flag (0 : OFF, 1 : ON)</p>

## CHSC\_PRE

Set the preset value of HSC

GM1	GM2	GM3	GM4	GM5	GM6
					●

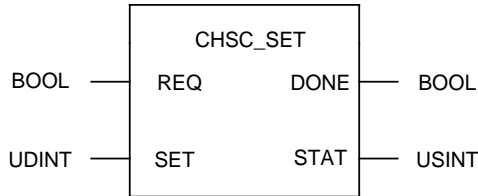
FUNCTION BLOCK	Description
 <pre> graph LR     subgraph CHSC_PRE         REQ[REQ]         PSET[PSET]         DONE[DONE]         STAT[STAT]     end     REQ --- CHSC_PRE     PSET --- CHSC_PRE     CHSC_PRE --- DONE     CHSC_PRE --- STAT             </pre>	<p><b>Input</b></p> <p>REQ : Request signal for F/B execution</p> <p>PSET : Set the preset value (0 ~ 16,777,215)</p> <p><b>Output</b></p> <p>DONE : Turns on after the F/B is executed with no error.</p> <p>STAT : Indicates the operation status of F/B</p>

- When the PRE\_I/E is set as 0 (Preset input by sequence program), the current value of HSC is changed as the assigned preset value with the rising edge of REQ input.
- When the PRE\_I/E is set as 1 (Preset input by external preset input), the current value of HSC is changed as the assigned preset value with the rising edge of external preset input. At this time, the REQ input of CHSC\_PRE is ignored.
- The CY output is set off while the CHSC\_PRE F/B is executing.
- The CHSC\_PRE F/B is disabled while the CT\_E input of CHSC\_WR F/B is 0 (Counter disabled).

## CHSC\_SET

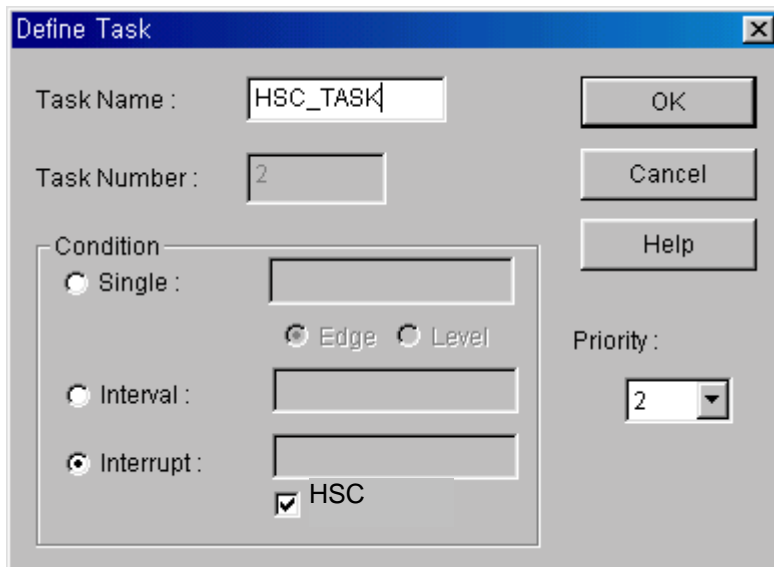
Assign a setting value to be compared with the current value of HSC

GM1	GM2	GM3	GM4	GM5	GM6
					●

FUNCTION BLOCK	Description
 <pre> graph LR     subgraph CHSC_SET         REQ[REQ]         SET[SET]         DONE[DONE]         STAT[STAT]     end     REQ --- BOOL1[BOOL]     SET --- UDINT[UDINT]     DONE --- BOOL2[BOOL]     STAT --- USINT[USINT]         </pre>	<p><b>Input</b> REQ : Request signal for F/B execution                  SET : Set a setting value (0 ~ 16,777,215)</p> <p><b>Output</b>                  DONE : Turns on after the F/B is executed with no error.                  STAT : Indicates the operation status of F/B</p>

Run a task program when the current value of HSC reaches to the setting value.

To run a task program, define a high speed counter task program as following figure, and write a task program.



16.5.2 Error code of F/B

The following table shows error codes appear at the STAT output.

<b>Error code</b>	<b>Description</b>
00	No error
01	Built-in high speed counter is not found (GM6-CPUA, GM6-CPUB CPU module)
02	Input data error at MULT input of CHSC_WR (2 Phase Mode□□ 1, 2, 4 □□□ □□□ □)
03	PSET (CHSC_PRE) or SET (CHSC_SET) is out of specified range (0 ~ 16,777,215).
04	Execute Preset command while the HSC is disabled status